EECS6321 Tutorial

HSPICE

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To Start with…

- Create your local directories for this course
  - $mkdir myexample
- Copy source codes from
  - /courses/ee6350/proj_2025Spring/ref/
  - $cp –rf /courses/ee6350/proj_2025Spring/ref/hspice/ ./myexample
- Sh files
  - run.sh
  - nuke.sh
- Please read the scripts line by line
- Please run your scripts at your local directories

Please change the followings

- hspice/inv/inv.sp

```
.subckt inv in out vdd vss
XP0 out in vdd vdd pfet l=0.12u w=1u nf=1
XN0 out in vss vss nfet l=0.12u w=0.5u nf=1
.ends
```

```
.subckt inv in out vdd vss
* XP0 out in vdd vdd pfet l=0.12u w=1u nf=1
* XN0 out in vss vss nfet l=0.12u w=0.5u nf=1
MP0 out in vdd vdd pch w=0.26u l=0.06u  nf=1
MN0 out in vss vss nch w=0.195u l=0.06u  nf=1
.ends
```

- hspice/inv/run.sp

```
** Library files **
.lib '/courses/ee6321/share/IBM_PDK/cmrf8sf/relDM/HSPICE/models/allModels.inc' tt
.include '/courses/ee6321/share/IBM_PDK/cmrf8sf/relDM/HSPICE/models/design.inc'
```

```
**** Include library
.include "../common_scripts/lib_tsmc65_gp.l"
```

HSPICE Netlist Structure

- Library files
  - TSMC 65nm MS RF GP technology
- Simulation options (Please refer to references)

```
**** Include library
.include "../common_scripts/lib_tsmc65_gp.l"

* General options
.option POST=1          $ Output format is binary
.option PROBE=1
.option MEASDGT=6
.option NUMDGT=6
.option DCSTEP=1
.option INGOLD=2
.option MEASOUT=1
.option PSF=1           $ Comment out if you want to use the CSCOPE
.option ARTIST=1
.option CAPTAB

* Spice accuracy options
.option METHOD=GEAR     $ Numerical integration method is used for a transient analysis
.option RELTOL=1e-6     $ Default: 1e-3
.option RUNLVL=6        $ Default: 3
.option GMINDC=1e-24
.option GMIN=1e-24
.option PIVTOL=1e-25
```

HSPICE Netlist Structure

- Components
  - ‘x_’ instantiates a subckt
  - ‘m_’ instantiates a transistor model
  - The following four nodes are net names of (D,G,S,B) in order
  - ‘r_’, ‘l_’, ‘c_’ are 2-node passive components
- When the sub-circuit size is huge, it is better to use the multiple subckt flies

```
.subckt inv in out vdd vss
* XP0 out in vdd vdd pfet l=0.12u w=1u nf=1
* XN0 out in vss vss nfet l=0.12u w=0.5u nf=1
MP0 out in vdd vdd pch w=0.26u l=0.06u  nf=1
MN0 out in vss vss nch w=0.195u l=0.06u  nf=1
.ends
```

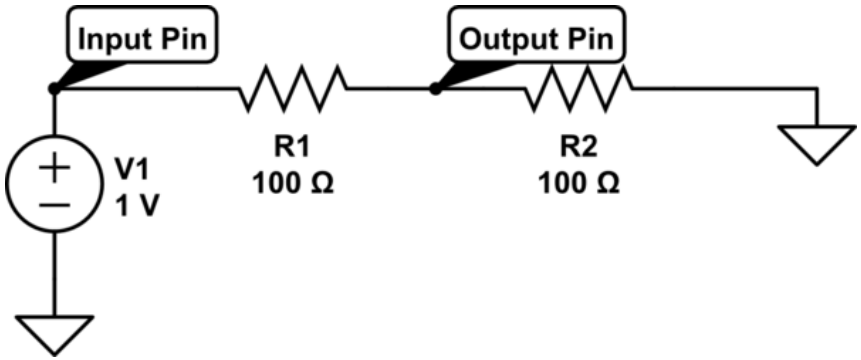
HSPICE Netlist Structure

- Parameter setting
- Sources
  - DC & AC: Vxxx n+ n- <DC=dcval> <AC=acmag, acphase>
  - PULSE: Vxxx n+ n- PULSE v1 v2 td tr tf pw period
  - PWL: Vxxx n+ n- PWL t1 v1 <t2 v2 t3 v3…> <R=repeat> <TD=delay>
- Analysis
  - DC analysis (.ms0)
  - AC analysis (.ma0)
  - Transient analysis (.mt0)
  - We can sweep some parameters, do Monte-Carlo simulation

```
41 ** Sourses **
42 .param par_vdd=1
43 .param t_rf=100p
44 vvdd    vdd     0   DC=par_vdd
45 vvss    vss     0   DC=0
46 vvin    in      0   pwl(0 0 10n 0 '10n+t_rf' par_vdd 20n par_vdd '20n+t_rf' 0)
47 cload   out     0   c=10f
48
49
50 ** Analysis **
51 .param simtime=30n
52 .tran 1p simtime START=0
53 .probe v(*)
```

HSPICE Netlist Structure

- Vector input helps to generate many digital inputs
- You can write a .vec file manually
- You can also generate it from a vcd file
  - You can generate a vcd using a dynamic Verilog simulator (e.g., Modelsim)
  - Example: /courses/ee6350/proj_2025Spring/ref/hspice/down_counter/vec_files



https://electronics.stackexchange.com/questions/572407/custom-varying-delays-on-a-hspice-digital-vector-file

```
r9 vout<4> 0 1e3
r8 v<4> vout<4> 1e3
r7 vout<3> 0 1e3
r6 v<3> vout<3> 1e3
r5 vout<2> 0 1e3
r4 v<2> vout<2> 1e3
r1 vout<1> 0 1e3
r0 v<1> vout<1> 1e3

.vec 'tabvec.vec'

.print v(*)
.probe v(*)
.options post

.tran 1n 200n
```

```
radix 1111
vname v<4> v<3> v<2> v<1>
io iiii
tunit ns
period 10
trise 0.01
tfall 0.01
vih 1
vil 0

0000
0001
0010
0011
```

HSPICE Netlist Structure

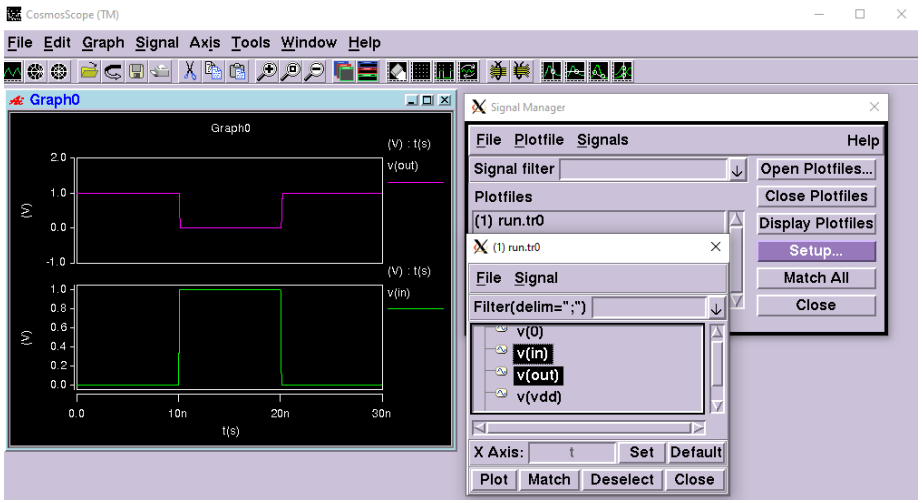
- Measurements
  - Rise, Fall, Delay
  - Average, RMS, Min, Max, & Peak-to-Peak
  - Find-When
  - Equation Evaluation
  - Derivative Evaluation
  - Integral Evaluation
  - Relative Error

```
56 ** Measurements **
57 .measure r_delay TRIG v(in) val='0.5*par_vdd' rise=1 TARG v(out) val='0.5*par_vdd' fall=1
```

How to Run HSPICE & See Results

- Run HSPICE
  - Command: $(time) hspice run.sp (> run.lis)
  - Using shell scripts: run_spice.sh, nuke.sh

- Verification tools
  - *.m**x**0 files
  - Cosmos Scope: $cscope
  - Virtuoso Visualization & Analysis (VIVA): $viva



Available Tutorials

- HSPICE
  - Getting Started with Hspice - Wisconsin-Madison
  - HSPICE & CosmosScope Tutorial
  - HSPICE User Guide – Synopsys
  - Digital vector file (vector_file)

End of Slides